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A Power Optimized Divide by N Prescaler Design on 50nm CMOS Process

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Abstract: In this paper divide by N prescaler counter is discuss. Instead of using conventional counter design technologies, a decision logic circuit is needed to generate predictable counting states. This circuit can be design by using transmission gate logic as a basic design cell. An initial module generates predictable counting states for higher significant bit modules through the state look-ahead path. In order to attain high operating frequency a high speed parallel counter is presented. In our work the counter operating frequency is varied by using a parallel counter architecture of transmission gate base flip-flops. The operation speed is improved by reduction of the critical path delay and the low power consumption can be achieved due to less number of interconnects. Simulation results in a standard 50nm CMOS process.

Keywords: Transmission Gate, Asynchronous Counter, D Flip-flop, Demultiplxer, Frequency synthesizer, Microwind.

I. INTRODUCTION

Frequency dividers are widely considered as a major limiting factor in frequency synthesizer systems, which require a very fast settling frequency feedback loop and a wide-range of frequency division ratios. Most modern frequency dividers are typically classified as cascaded asynchronous programmable prescaler counters, programmable swallow counters, or programmable divide-by-N counters. The cascaded asynchronous programmable prescaler counter offers a high operating speed due to the absence of a long delay loop [3]. The frequency prescaler is the basic module of phase lock loop (PLL). Its operating frequency is large with high power dissipation. Thus the power dissipation, switching speed and frequency divider generation is the key concern of design. In this work the structure of counter compose of three simple CMOS logic modules. An initial module generates predictable counting states for higher significant bit modules through the state look- ahead path. In order to attain high operating frequency a high speed parallel counter is presented. In our work the counter operating frequency is varied by using a parallel counter architecture of pass transistor base flip-flops.

II. RELATED WORK

In [1] a novel extended true single-phase clock-based divide-by-3/4 prescaler is presented. Their proposed prescaler was designed under 0.18 um CMOS process. The prescaler operates in divide-by-3 and divide-by-4 mode when the signal MC is '0' and '1', respectively. The designed prescaler adds only two PMOS transistors to the conventional divide-by-4 divider to control the divide mode and reduces the total number of the transistors to 16. Therefore, the power consumption of the proposed prescaler is decreased. The critical path delay is reduced by combining the logic gates with the stage of DFF [1]. In [2] divide-by-2/3 counter design for low supply voltage and low power consumption applications is discussed. They work on low supply voltage operations, the voltage range of simulations is between 0.6 and 0.9 V in contrast to the nominal 1.8 V used in 0.18 um technology. The design was successfully simplifies the control logic and one PMOS transistor alone serves the purposes of both mode select and counter excitation logic. The circuit simplicity leads to a shorter critical path and reduced power consumption.
The paper [3] design a scalable high-speed divide-by-N frequency divider using only basic digital CMOS circuits. The parallel counter is based on a state look-ahead component in conjunction with an internal pipeline structure in order to simultaneously trigger all state value updates without a rippling effect. In paper [3] they implemented a divider using a 0.15-µm CMOS design process and achieved a maximum operating frequency of 2 GHz, an area of 112 848 µm2 (900 transistors), and consumed 15.47 mW of power dissipation.

III. INTRODUCTION OF PARALLEL COUNTER ARCHITECTURE

A register that goes through a prescribed sequence of states upon the application of input pulses is called a counter. The input pulses may be clock pulses, or they may originate from some external source and may occur at a fixed interval of

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time or at random. The sequence of states may follow the binary number sequence or any other sequence of states. A counter that follows the binary number sequence is called a binary counter. An n-bit binary counter consists of n flip-flops and can count in binary from 0 through 2^n - 1. Counters are available in two categories: ripple counters and synchronous counters. In a ripple counter, a flip-flop output transition serves as a source for triggering other flip-flops. In other words, the C input of some or all flip-flops are triggered, not by the common clock pulses, but rather by the transition that occurs in other flip-flop outputs. In a synchronous counter, the C inputs of all flip-flops receive the common clock. A binary asynchronous counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the C input of the next higher order flip-flop. The flip-flop holding the least significant bit receives the incoming count pulses. The address generation for data read and write memory data, branching and storage functions in Microprocessors, microcontrollers and application-specific processors, Incrementer Decrementer logic is use. The circuit can be design by using low power high speed adders and a toggle flip-flop base asynchronous counter logic circuit. The output of counter is connected to the one of the bit of adder unit and the second input of adder unit is connected through a chain of XOR logic to get 2's complement number to add or subtract the counter output. The second input can be act as a load value for the circuit. The input given on second input is consider as a load value and the circuit either increment or decrement from this load value depends on the direction signal 'INCDEC' from the logic circuit. The Parallel counter is design with three basic modules consists of flip-flops and extra logic, which determines the next state of counter. The counter structure consists of the these design modules counts succeeding states through a fixed set of preassigned count states of which each subsequently count state represents the successive counter value in a chain.

The transmission gate base counter design modules consist of three modules called as adder module, latch module, and counter module. This module determines the next state of counter depends on the present state i.e. design modules counts succeeding states through a fixed set of pre-assigned count states, of which each subsequently count state represents the successive counter value in a chain.

Fig. 1 shows the block diagram for different frequency generation using demultiplexer as a clock generator. The input clock of multiplexer module is connected to the different counter circuits through transmission gate base de-multiplexer. This logic can be extended for more divide by N counter using higher size demultiplexer logic.

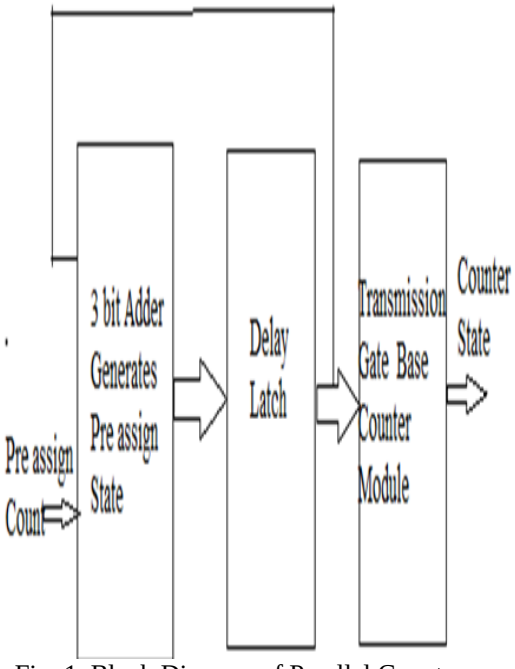

Fig. 1. Block Diagram of Parallel Counter.

The 16 states counter module is design with a transmission gate base multiplexer logic circuit which work as a 16 states counter logic. The purpose of this module is to create all counter in a predefined ordered position and it enable future states in successive module-2 in conjunction with stimulus from the module-3. This counter counts the next state when a stimulus from the state module 2 four bit latch. The module 1 of 16 states counter design by using transmission gate counts the successive step and the module 2 generates future step size of counting sequence and thus organizes the counting path for these future states. Module 3 is design using 4 bit ripple carry adder in order to decode the low-order count states and carries this decoding over several clock cycles in order to trigger high-order count states. The present state of module 2 is added with the step size input and the next state sequence is generates from module 2.

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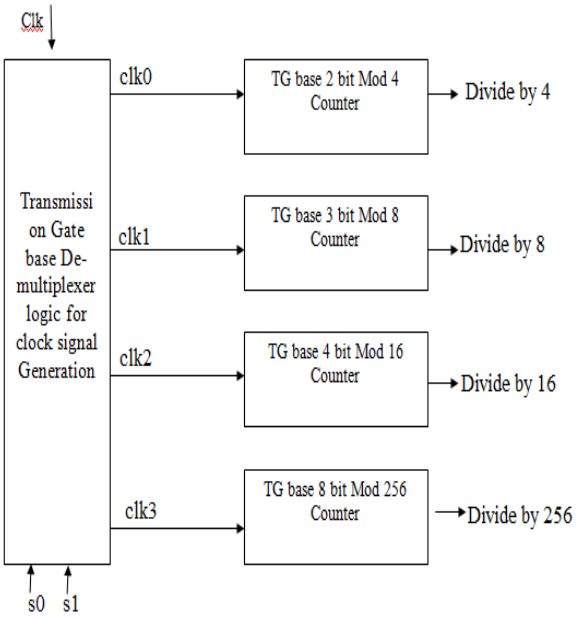

Fig. 2. Block Diagram for Selection logic base different Divide by N counter

Our design counter circuits can be built using T flip-flops because the toggle feature is naturally suited for the implementation of the counting operation. We can design this flip-flop by connecting the Qn output to the D input of Master slave D flip-flop shown in figure. Fig. 2 shows four bit counter capable of counting from 0 to 15. The clock inputs of the four flip-flops are connected in cascade. The input of each flip-flop will be toggled at each negative edge of its clock. We are assuming that the purpose of this circuit is to count the number of pulses that occur on the primary input called Clock. Thus the clock input of the first flip-flop is connected to the Clock line. The other three flip-flops have their clock inputs driven by the Q output of the preceding flip-flop. Therefore, they toggle their state whenever the preceding flip-flop changes its state from Q = 1 to Q = 0, which results in a positive edge of the Q signal.

IV. IMPLEMENTATION LOGIC DESIGN FLOW

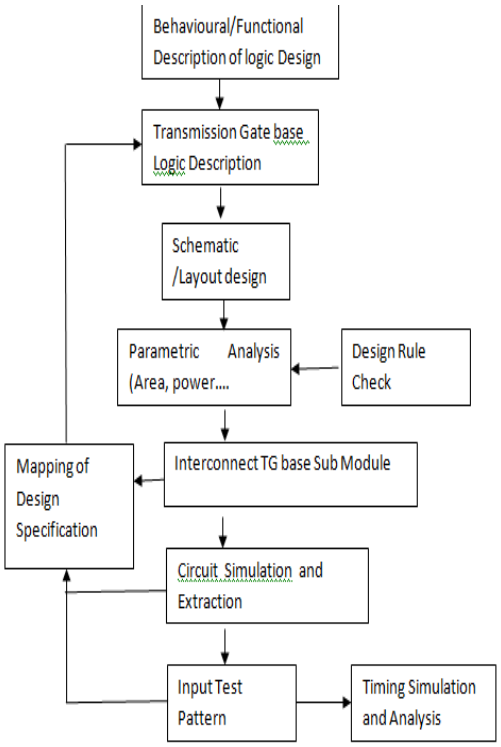

Fig. 3. Design Flow

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Functional description is primarily studied and the structure of the digital IC circuit to be designed. Behavioural description is then formed to analyse the design in terms of functionality, performance, compliance to given principles, and other specifications. RTL description is made by the use of Microwind layout editor tool. This layout description is simulated to analysis functionality. From here forwards work needs the help of layout simulator tools. A gate-level layout is a description of the circuit in terms of gates and inter connections between them, which are made in such a manner that they meet the timing, power and area specifications. At last a physical layout is made, which will be verified and then transmit to fabrication.

The mask layout of the typically design flow is shown in Fig. 3. The physical mask layout design of CMOS logic procedure begin with the circuit topology to take in the desired logic function and the initial sizing of the transistor at the base of number of devices and the length of interconnection. A simple poorly diagram can be drawn, viewing the location of the transistor, the local interconnection among the transistor and the location of contacts. After that a possible mask layout is drawn using layout editor tool according to the layout design rule. Next the final design rule check (DRC), a circuit extraction process to find out the real transistor size. The layout modification is generally determined on the width to length ratios of transistor, since it set up the transistor size, parasitic capacitances.

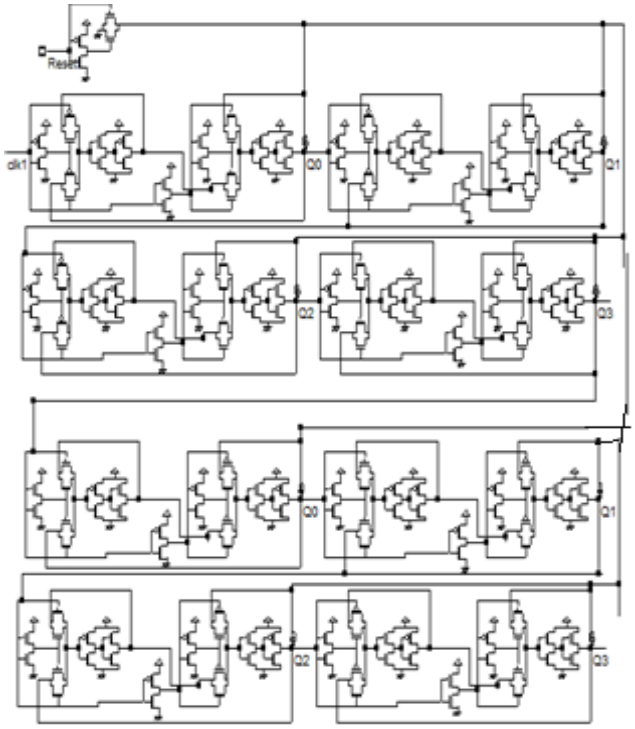

Fig. 4. Eight bit Asynchronous Counter using transmission gate.

Fig. 4 shows the schematic of 8 bit transmission gate base counter. In consist of 32 transmission gates and 56 NOT logic gates. The total 88 NMOS and 88 PMOS transistors. A one transmission gate along with inverter is use to reset the content of counter. The output of this reset logic circuit is connected to the output port Q of each flip-flops and the input of its transmission gate is connected to ground supply. On the arrival of reset signal the reset TG is turn ON and the output of each flip flop is connected to the ground supply through this reset circuit. When the reset signal is inactive, then the counter starts to increment its state at each negative edge trigger of clock signal.

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